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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,134	07/25/2001	Clifford Zitlaw	400.122US01	6437

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EXAMINER	
CHACE, CHRISTIAN	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/915,134	ZITLAW ET AL.	
	Examiner	Art Unit	
	Christian P. Chace	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action has been issued in response to amendment filed 28 March 2005. Claims 1-38 are pending. Applicants' arguments have been carefully and respectfully considered, but they are not persuasive. Accordingly, this action has been made FINAL.

Drawings

Figure 5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance. See paragraph 39 of the instant specification, which refers to the "older systems such as the system 500 of figure 5."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 4-10, 12-14, 17-20, 22-31, and 33-36 are rejected under 35 U.S.C. 102(a) as being anticipated by applicants' admitted prior art.

With respect to independent claims 1, 8, 17, 22, and 28, a synchronous flash memory device is disclosed in paragraph 7 of the instant specification.

A memory array is disclosed in prior art figure 1, #106.

A control circuit is disclosed in prior art figure 1, #100.

A synchronous memory interface is disclosed in paragraph 7. The synchronous flash memory device beginning initialization upon receiving a power signal (RP#) on a power bus (signals are inherently delivered on a bus) is disclosed in paragraph 28 and in prior art figure 2. Stopping the initialization in response to an external command is inherent in the prior art figure 2 – a computer must be told what to do. Therefore, an "external command" must be issued to stop the initialization.

With respect to claim 4, the synchronous [memory] interface being an SDRAM or a DDR-SDRAM compatible interface is disclosed in figure 2.

With respect to claims 5, 12, 18, and 23, the initialization cycle beginning when the power signal on the bus reaches a predefined "trip point," is disclosed in figure 2 as "t.sub.0"

With respect to claims 6 and 13, the initialization cycle beginning "a redefined time period" after receiving the power signal on the bus is disclosed in figure 2 as "t.sub.0," with the predefined time period being zero – it starts immediately.

With respect to claims 7, 14, and 25, the initialization cycle stopping at "a random point" in the initialization cycle when the external command is received is disclosed in figure 2, with the "random point" being when it is complete (t.sub.1).

With respect to claims 9-10 and 26-27, the memory device being a non-volatile memory device (specifically, a flash memory) is disclosed in figure 1, #106.

With respect to claims 19 and 24, beginning the initialization cycle upon receiving the power signal further comprising beginning the initialization cycle upon the power signal reaching a predetermined value is disclosed as discussed supra with respect to claims 6 and 13. The delay period is zero.

With respect to claim 20, the initialization signal stopping upon receiving the command further comprises stopping the initialization signal at an "in-progress point" in the cycle is disclosed as discussed supra with respect to claims 7 and 14.

With respect to claim 29, a separate external data source is disclosed in figure 5, #508.

With respect to claim 30, the separate external data source further comprising a non-volatile memory device is disclosed in figure 5, #508. Note the description in paragraph 39 referring to the system of figure 5 as old.

With respect to claim 31, the separate external data source being coupled to the host controller on a separate bus is also disclosed in figure 5.

With respect to claim 33, the host controller receiving software routines to control the synchronous flash memory device from a non-volatile data source is disclosed in paragraph 39.

With respect to claim 34, the non-volatile data source being [storing] a BIOS is disclosed in figure 5. Examiner wishes to note herein that BIOS is not a physical memory – it is usually stored on a ROM, but can moved to RAM to operate faster upon POST. Accordingly, while examiner knows what applicants mean here, it is strongly suggested that the instant wording be rearranged to be consistent with terminology known in the art.

With respect to claim 35, the host controller stopping the initialization cycle by issuing an external command is disclosed in paragraph 39.

With respect to claim 36, the host controller comprising a processor is disclosed in figure 5, #502.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 37-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Kessler (US Patent #6,820,196 B2).

With respect to independent claims 37 and 38, a computer system is disclosed in the title.

A processor is disclosed in figure 1, #12.

A memory device coupled to the processor is disclosed as the flash in figure 1, #14. The memory device beginning an initialization cycle is disclosed in figure 1, #22 and figure 3. Doing so in response to Vcc is disclosed in figure 1, #10. Terminating the

initialization cycle in response to the processor (examiner assumes applicants mean a command from the processor) is disclosed in figure 3, #22-3 as terminating the timeout.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3, 11, 21, and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art in view of SGS-THOMSON ST10F166.

Applicants' admitted prior art discloses all of the claimed limitations as discussed supra with respect to the independent claims and the intervening claims upon which the instant claims depend, not repeated herein in the interest of an efficient Office action.

The difference between applicants' admitted prior art and the instant claims, however, is the explicit recitation that the external command is received through the synchronous interface and is a STOP command.

However, the SGS-THOMSON reference discloses, on page 5 at the bottom of the page, an EINIT instruction being executed in the synchronous flash device. An instruction is a command. The pins are the "synchronous interface" and the EINIT command is an end of initialization command, or "STOP."

Therefore, it would have been obvious to one of ordinary skill n the art at the time o the invention, to utilize the STOP command of SGS-THOMSON as the external command of applicants' admitted prior art, because the MCU of SGS-THOMSON MCU

device offers a plurality of benefits, as shown on page 1, that would readily appreciated by one of ordinary skill in the art, such as the Idle and power-down modes, for example, which save power, as made hackneyed in the state of the art.

Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art.

Applicants' admitted prior discloses the claim limitation so the claims upon which the instant claim depends, as discussed supra.

The difference between the instant claim and applicants' admitted prior art is the explicit recitation that the separate bus is a non-synchronous bus.

However, one of ordinary skill in the art would appreciate the benefits and costs associated with synchronous and non-synchronous (asynchronous or isochronous) busses in a computer system. As this particular bus is disclosed to have a particular purpose or be for any reasons whatsoever non-synchronous, use of same is merely an issue of design choice, and would have been obvious to one of ordinary skill in the art at the time of the invention, and as admitted by applicants in the instant remarks at page 5, having the teachings of applicants' admitted prior art before him/her, because, for example, in an asynchronous device, the operations may proceed independent of any timing signal, thereby executing faster than a timed program, as made hackneyed in the state of the art.

Response to Arguments

With respect to applicants' arguments that figure 5 is not admitted prior art, as discussed at page 4 of the instant remarks, in particular because system 500 is shown as incorporating a synchronous Flash memory device 506. However, at page 5 of the instant remarks, with respect to claim 32 in particular, applicants state that, "...various forms of memory devices and busses, including synchronous and asynchronous memory devices and busses, are well known in the art." Accordingly, the objection has been maintained.

With respect to applicants' argument that the title is, indeed, descriptive, examiner agrees, and has removed the objection. The remaining objections to the specification have been removed as well, in light of the instant amendment.

With respect to applicants' argument that applicants are allowed to rely upon the knowledge of one skilled in the art for written description and enablement, and that the subject matter of claim 32 is well-known in the art, examiner agrees, and has removed the rejection.

With respect to applicants' argument that the rejection of claims 1, 4-10, 12-14, 17-20, 22-31, and 33-36 is improper under 35 USC 102(b), examiner agrees, and apologizes for any inconvenience as a result of this typographical error. Examiner has corrected the error, and properly noted that the claims are, indeed, rejected under 35 USC 102, but under subsection (a), not (b).

With respect to applicants' arguments that, "... paragraph 28 of the present application describes that the #RP signal is 'reset' or 'power down' signal that is

'released 202 by a compatible synchronous host controller (not shown) after power-up,' and is therefore not a power signal on a power bus as maintained by examiner." Examiner respectfully disagrees – a "power down" signal is, indeed, reasonably interpreted as a "power signal." The bus a power signal is delivered on may reasonably be considered a "power bus." Finally, a command must, inherently, be issued at some point to stop the initialization cycle. (Applicants to not claim what the command is "external" to, so examiner has reasonable interpreted "external" to be anything other than the actual memory cells themselves.) The claim language, as it stands, is very broad, and may be reasonably interpreted much more broadly than applicants appear to assert instantly.

With respect to applicants' arguments at the bottom of page 9 of the instant remarks, and into page 10, that because Kessler, "selectively initializes the contents of an internal Flash memory device upon power up," Kessler does not teach or suggest, "...a synchronous Flash memory that begins an initialization cycle upon power-up and stops the initialization cycle in response to an external command." Examiner respectfully disagrees, and again refers applicants to the inherency of a command of some sort at some time that must be given to stop the initialization. If, for example, the initialization stops after a period of time, that period of time must have been programmed in (issued, given) at some point, via the processor, e.g.

With respect to applicants' arguments that combining the elements of the AAPA with the ST10F166 document, examiner respectfully disagrees, and refers applicants to the rejection supra.

With respect to applicants' argument that claim 32 is allowable, examiner refers applicants to their remarks on page 5 of the instant remarks, which state that the subject matter of claim 32 is well-known to those of ordinary skill in the art, as discussed supra.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian P. Chace whose telephone number is 571.272.4190. The examiner can normally be reached on MAXI FLEX.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571.272.4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christian P. Chace
Primary Examiner
Art Unit 2189